a second p-doped well disposed within the doped epi silicon layer; and

an n-doped well disposed within the doped epi silicon layer, wherein the second p-doped well and the n-doped well are coupled together.

2. The CMOS device of claim **1**, further comprising a phase-change material coupled to a diode, wherein the diode is coupled to the n-doped bitline.

3. The CMOS device of claim **1**, further comprising a non-volatile memory array coupled to the n-doped bitline.

4. The CMOS device of claim **3**, wherein the memory array includes diodes.

5. The CMOS device of claim **4**, wherein the diodes comprise epi-silicon.

6. The CMOS device of claim **5**, wherein the non-volatile memory array includes a phase-change material.

7. The CMOS device of claim **6**, wherein the phase-change material comprises a Chalcogenide alloy.

8. The CMOS device of claim **7**, wherein the substrate is P^+ doped and wherein the doped epi silicon layer is P^- doped.

9. The CMOS device of claim **6**, wherein the phase-change material comprises one or more of germanium, tellurium and antimony.

10. The CMOS device of claim **9**, wherein the substrate is P^+ doped and wherein the doped epi silicon layer is P^- doped.

11. The CMOS device of claim **10**, further comprising a NMOS transistor coupled to the second p-doped well.

12. The CMOS device of claim **11**, further comprising a PMOS transistor coupled to the n-doped well.

13. The CMOS device of claim **1**, wherein the non-volatile memory array includes a phase-change material.

14. The CMOS device of claim **13**, wherein the phase-change material comprises a Chalcogenide alloy.

15. The CMOS device of claim **14**, wherein the substrate is P^+ doped and wherein the doped epi silicon layer is P^- doped.

16. The CMOS device of claim **15**, wherein the phase-change material comprises one or more of germanium, tellurium and antimony.

17. The CMOS device of claim **16**, wherein the substrate is P^+ doped and wherein the doped epi silicon layer is P^- doped.

18. The CMOS device of claim **17**, further comprising an oxide layer disposed on a polysilicon gate that is coupled to the n-doped bitline.

19. The CMOS device of claim **18**, further comprising a non-volatile memory array coupled to the oxide layer.

20. The CMOS device of claim **19**, wherein the memory array includes diodes.

* * * * *